IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Toshiyuki UETAKE**

Serial Number: **Not Yet Assigned**

Filed: **July 7, 2003**

For: **SEMICONDUCTOR STORAGE DEVICE WITH SIGNAL WIRING LINES RMED ABOVE MEMORY CELLS**

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 7, 2003

Sir:

In compliance with 37 CFR 1.56, Applicant calls to the attention of the Patent and Trademark Office the reference listed on the attached PTO-1449.

A copy of the reference is enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

William L. Brooks
Attorney for Applicant
Reg. No. 34,129

WLB/jaz
Atty. Docket No. **030705**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: PTO-1449; References (**1**)

INFORMATION DISCLOSURE STATEMENT PTO-1449	Atty. Docket No. **030705**	Serial No. **New Application**
	Applicant(s): **Toshiyuki UETAKE**	
	Filing Date: **July 7, 2003**	Group Art Unit: **Not Yet Assigned**

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA						
_____	AB						
_____	AC						
_____	AD						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Translation (Yes or No)
_____	AE	9-74172	03/18/97	Japan	Yes-Abstract and Partial
_____	AF				
_____	AG				
_____	AH				
_____	AI				

OTHER DOCUMENTS

_____	AJ	
_____	AK	

Examiner	Date Considered

[0045]

Fig. 9 is a diagram showing the main structure of a RAM macro B31 according to a fourth embodiment of the invention. Fig. 4(A) is a plan view showing the main area of the RAM macro B31, and Fig. 4(B) is a cross sectional view showing the main region of the RAM macro B31. In Figs. 4(A) and 4(B), identical constituent elements to those shown in Fig. 8 are represented by using identical reference numerals and the description thereof is omitted.

[0046]

The RAM macro B31 constitutes SRAM and the like. Various elements such as cells are formed on the semiconductor substrate 2 and are covered with an insulating layer 8 of an oxide film, a nitride film or the like. Disposed on the insulating layer 8 are word lines WL for transferring word signals. The word lines WL are covered with an insulating layer 44. Disposed on the insulating layer 44 are bit lines BL for transferring small signals. Disposed in the same layer as that of the bit lines BL are first shield lines SL1 for shielding the right and left sides of the bit lines BL.

[0047]

An insulating layer 45 covers the bit lines BL and first shield lines SL1. Data busses 42 are disposed on the insulating layer 45. The data busses 42 are pass-wires which pass above the RAM macro 31 and

interconnect the RAM macro B32 and RAM macro B33. The data bus 42 is disposed in parallel to and above the corresponding underlying first shield line SL1. In the same layer as that of the data busses 42, second shield lines SL2 are disposed in parallel to and above the corresponding and underlying bit lines BL to shield the upper sides of the bit lines BL. The second shield line SL2 has a wiring width wider than that of the bit line or lines BL and overlaps the first shield lines SL1 disposed on the right and left sides of the bit line or lines BL.

[0048]

The first and second shield lines SL1 and SL2 are made of aluminum, tungsten, copper or the like and fixed to a ground level, a power source level, a reference level or the like. An insulating film 46 covers the data busses 42 and second shield lines SL2. Data busses 43 are disposed on the insulating film 46. The data busses 43 are pass-wires which pass above the RAM macro 31 and interconnect the RAM macro B34 and RAM macro B35. A passivation layer 47 is formed covering the data busses 43.

[0049]

In this embodiment, the first and second shield lines SL1 and SL2 are disposed in parallel to the bit lines BL to which small amplitude signals are supplied. The first and second shield lines SL1 and SL2 are disposed surrounding the right and left sides and upper side of the bit line or lines BL, and fixed to a constant level. The first and second shield lines SL1 and SL2 shield and protect the bit lines BL from the data busses

42 and 43 disposed above the bit lines BL.

[0050]

In this embodiment, since the first and second shield lines SL1 and SL2 are formed in the same layers as those of the bit lines BL and data busses 42, the bit lines can be formed at the same time when the data busses 42 are formed, so that specialized processes of forming the bit lines BL and data buses 42 are not necessary. The data busses 43 can be disposed at any positions above the RAM macro B31 because the data busses 43 are not influenced by the wiring direction of the first and second shield lines SL1 and SL2.

[0051]

As described above, according to this embodiment, the data busses 42 and 43 can be passed above the bit lines BL to which small amplitude signals of the RAM macro B31 are transferred. The data busses 42 and 43 can thus be disposed along straight lines so that a signal delay can be minimized as much as possible.